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# N-Bit CMOS Comparator Using Parallel Prefix Tree

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**ABSTRACT**

It provides new comparator model gives large range experience, with faster operation by converting Digital CMOS cells. This comparator make use of N-bit scalable parallel prefix constructs strategic advantage of comparison from the MSB towards the LSB by bit by bit comparing as there are equal by setting the status bit. The advantages of these comparators are high speed and low power for a wide range. The design uses the standard VLSI design that can be varied for logical derivations of delay as the role of bandwidth range. HSPICE model for 32 bit comparator shows defective case input and output delay of 0.86ns at most power wastage of 7.7mW.

**KEY WORDS:** N Bit CMOS, ALU, Comparator.

## 1. INTRODUCTION

The Comparators are design for applications such as comparison computation, test circuit applications and optimized equality comparators processor components for general purpose. The comparator logic design uses of comparators in high performance system and low power consumption as its greater importance on performance.

**Comparator Architectural Overview:** The comparison resolution module is shown the figure 1 which is in the parallel prefix tree structure that is from the MSB to LSB that can be operates in the bit wise operations that is to be two operands of N bit of A and B, which the bits are denoted by the N-1 logics of operations that is from the MSB to LSB bit of operations.

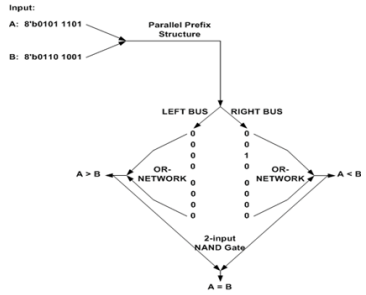



**Figure.1. Bit position Example**

The 8 bit comparison of inputs with the bit position of A is equal to 01011101 and B is equal to 01101001 is shown in the Fig. 1. The comparison module terminates the following bits since it is from the MSB to LSB.

**Table.1. Symbols in the Logic Circuit**

| Denoted | Explain |
|---|---|
| *N* | N bits |
| *A* | Inputs |
| *B* | Inputs |
| *R* | Buses |
| *L* | Buses |
| & | AND |
| \| | OR |

The partition structure into five prefixing sets are the table 1 and table 2, the set performance the specific function that each bit performances whose outputs saved as the input for the next level of bit positions until the next set up to the fifth bit position of operations to the two buses before the decision module. The parallel prefix structure that the components of number of inputs and number outputs with the maximum number of fan in and fan out which will the bit elimination after the bit position scarifications of signals , the operating speed can be improved and power can be reduced to greater part. The OR network with the fan in and fan out is limited by 4 bit partitioning of group of inputs of each bus.

**Comparator Design Details:** The Comparator design which shown the figure 2 which is based on the parallel prefix structure the comparator is designed. The table 1 and table 2 show the symbols definitions. The each bit of operations are said to be the group of cells which is used to produce the serve of bit positions with exceptions of bit sets that set I compare N bit of input A and input B which is in single bit operations level of execution N bit positions of computations the termination flags has that the cell computes for each of four flags of cell positions that provides functions to be similar to that of NOR logic is performed to continue.

**Table.2. Bit Comparator for Cell outcome**

| Cell Type | Input Driving -Type Cell Output |
|---|---|
| $Y_{15}$ | $D_{15}$ |
| $Y_{14}$ | $D_{15}\ D_{14}$ |
| $Y_{13}$ | $D_{15}\ D_{14}\ D_{13}$ |
| $Y_{12}$ | $D_{15}\ D_{14}\ D_{13}\ D_{12}$ |
| $Y_{11}$ | $C_{3,0}\ D_{11}$ |
| $Y_{10}$ | $C_{3,0}\ D_{11}\ D_{10}$ |
| $Y_{9}$ | $C_{3,0}\ D_{11}\ D_{10}\ D_{9}$ |
| $Y_{8}$ | $C_{3,0}\ D_{11}\ D_{10}\ D_{9}\ D_{8}$ |
| $Y_{7}$ | $C_{3,1}\ D_{7}$ |
| $Y_{6}$ | $C_{3,1}\ D_{7}\ D_{6}$ |
| $Y_{5}$ | $C_{3,1}\ D_{7}\ D_{6}\ D_{5}$ |
| $Y_{4}$ | $C_{3,1}\ D_{7}\ D_{6}\ D_{5}\ D_{4}$ |
| $Y_{3}$ | $C_{3,2}\ D_{3}$ |
| $Y_{2}$ | $C_{3,2}\ D_{3}\ D_{2}$ |
| $Y_{1}$ | $C_{3,2}\ D_{3}\ D_{2}\ D_{1}$ |
| $Y_{0}$ | $C_{3,2}\ D_{3}\ D_{2}\ D_{1}\ D_{0}$ |

The Set 1 has the Ex Nor logic function with set 3 and set2 are NOR logic functions that to be used of the comparison of two inputs which to the given to the set 1 directly with set 2 and set 3 are consists of the status signals that are of control signals. From the set 3 the inputs to the set 4 which is of another NOR logic functions with the set 5 to the Multiplexers functions are used for the set 5 which will completes the operation of the comparison resolution module and it is given to the decision module which consists of OR network and network.

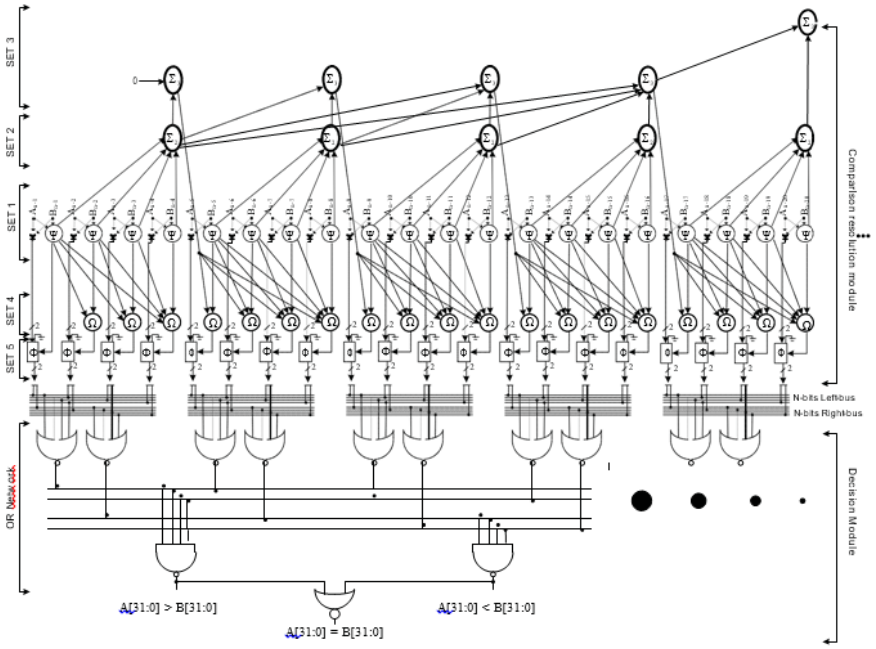
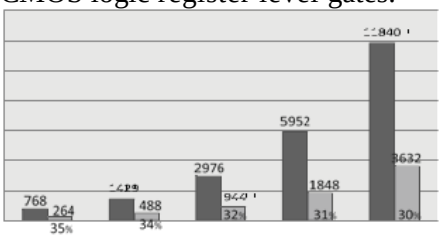



**Figure.2. Implementation details for the comparison resolution module and the decision module**

**Area, speed and power evaluations:**

The area, speed, and power evaluations of this comparator are evaluated for the N net-list comparator based on CMOS logic register level gates.



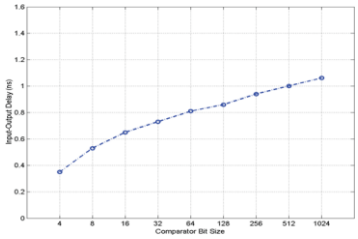



**Figure 3. Number of transistors with active transistors**

**Figure 4. Maximum in/out delay verses input bit width**

## 2. CONCLUSION

This paper explained about N bit comparator which will used for low power digital circuits. Here using two module are comparison module and decision module. The repeated bits of operations are in the single stage of logic circuits with two set of operations with maximum number of inputs and outputs. Fan in takes to be five and Fan out are to be four which are independent of input bit widths for the continuous technology leveling and logics to synthesis.

## REFERENCES

Abdel-Hafeez S, Single rail domino logic for four-phase clocking scheme, U.S. Patent 6 265 899, 2001.

Brintha Rajakumari S, Nalini C, An efficient data mining dataset preparation using aggregation in relational database, Indian Journal of Science and Technology, 7, 2014, 44-46.

Ercegovac M.D and Lang T, Digital Arithmetic, San Mateo, CA, Morgan Kaufmann, 2004.

Glass K.W, Digital comparator circuit, U.S. Patent, 5, 1992, 260- 680.

Guangjie W, Shimin S and Lijiu J, New efficient design of digitalcomparator, in Proc 2nd Int Conf Appl Specific Integr Circuits, 1996, 263–266.

Helms H.L, High Speed (HC/HCT) CMOS Guide. Englewood Cliffs, NJ, Prentice-Hall, 1989.

Jayalakshmi V, Gunasekar N.O, Implementation of discrete PWM control scheme on Dynamic Voltage Restorer for the mitigation of voltage sag /swell, 2013 International Conference on Energy Efficient Technologies for Sustainability, ICEETS, 2013, 1036-1040.

Kaliyamurthie K.P, Parameswari D, Udayakumar R, QOS aware privacy preserving location monitoring in wireless sensor network, Indian Journal of Science and Technology, 6 (5), 2013, 4648-4652.

Kaliyamurthie K.P, Udayakumar R, Parameswari D, Mugunthan, S.N, Highly secured online voting system over network, Indian Journal of Science and Technology, 6 (6), 2013, 4831-4836.

Khanaa V, Thooyamani K.P, Saravanan T, Simulation of an all optical full adder using optical switch, Indian Journal of Science and Technology, 6 (6), 2013, 4733-4736.

Khanaa V, Thooyamani K.P, Using triangular shaped stepped impedance resonators design of compact microstrip quad-band, Middle - East Journal of Scientific Research, 18 (12), 2013, 1842-1844.

Kumaravel A, Dutta P, Application of Pca for context selection for collaborative filtering, Middle - East Journal of Scientific Research, 20 (1), 2014, 88-93.

Norris D, Comparator circuit, U.S. Patent, 5, 1995, 534-844.

Raj M.S, Saravanan T, Srinivasan V, A modified direct torque control of induction motor using space vector modulation technique, Middle - East Journal of Scientific Research, 20 (11), 2014, 1572-1574.

Saravanan T, Raj M.S, Gopalakrishnan K, VLSI based 1-D ICT processor for image coding, Middle - East Journal of Scientific Research, 20 (11), 2014, 1511-1516.

Sengottuvel P, Satishkumar S, Dinakaran D, Optimization of multiple characteristics of EDM parameters based on desirability approach and fuzzy modeling, Procedia Engineering, 64, 2013, 1069-1078.

SN7485 4-bit Magnitude Comparators, Texas Instruments, Dallas, TX, 1999.

Sundararajan M, Optical instrument for correlative analysis of human ECG and breathing signal, International Journal of Biomedical Engineering and Technology, 6 (4), 2011, 350-362.

Thamotharan C, Prabhakar S, Vanangamudi S, Anbazhagan R, Anti-lock braking system in two wheelers, Middle - East Journal of Scientific Research, 20 (12), 2014, 2274-2278.

Udayakumar R, Khanaa V, Saravanan T, Saritha G, Retinal image analysis using curvelet transform and multistructure elements morphology by reconstruction, Middle - East Journal of Scientific Research, 16 (12), 2013, 1781-1785.

Uyemura J.P, CMOS Logic Circuit Design, Norwood, MA, Kluwer, 1999.

Vanangamudi S, Prabhakar S, Thamotharan C, Anbazhagan R, Design and fabrication of dual clutch, Middle - East

Journal of Scientific Research, 20(12), 2014, 1816-1818.

Vanangamudi S, Prabhakar S, Thamotharan C, Anbazhagan R, Design and calculation with fabrication of an aero hydraulwicclutch, Middle - East Journal of Scientific Research, 20 (12), 2014, 1796-1798.